

Substitute for form 1449A/PTO

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

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| Application Number | 09/956,903 |
| Filing Date | September 21, 2001 |
| First Named Inventor | FLETCHER, Thomas |
| Group Art Unit | 2816 8124 |
| Examiner Name | Not assigned Chat Do |
| Attorney Docket Number | 2207/11270 |

U.S. PATENT DOCUMENTS

| Examiner Initials * | Cite No. ¹ | Document Number Number - Kind Code ³ (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---------------------|-----------------------|---|--------------------------------|---|---|
| CD | | 6,208,907 B1 | 03/27/2002 | DURHAM et al | |
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| Examiner Initials * | Cite No. ¹ | Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ³ (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | T ⁶ |
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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| Examiner Initials * | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| CD | | Yee et al, "Clock-Delayed Domino for Dynamic Circuit Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 4, August 2000, pp 425-430 | |
| CD | | Yee et al, "Clock-Delayed Domino for Adder and Combinational Logic Design", IEEE, 1063-6404/96, pp 332-337, 1996 | |
| CD | | Jung, Perepelitsa, Sobelman, "Time Borrowing in High-Speed Functional Units Using Skew-Tolerant Domino Circuits," Proceedings, IEEE International Symposium on Circuits and Systems, pp. V-641 - V-644, 2000 | |
| CD | | Presentation by Carl Sechen dated March 17, 2000. <i>Output Prediction Logic: A high performance CMOS Design Technique</i> | |
| CD | | Taub, <i>Digital Circuits and Microprocessors</i> , pages 205-212, McGraw-Hill, 1982 | |

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|--------------------|--|-----------------|---------|
| Examiner Signature |  | Date Considered | 8/21/04 |
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| | | JP 5-259893 - Furuki (Abstract JP405-259893A) | 10/8/93 | Furuki | | |
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|---------------------|-----------------------|---|----------------|
| CD | | Related U.S. Patent Application Serial No. 10/020,447, filed December 18, 2001 | |
| CD | | Related U.S. Patent Application Serial No. 09/892,565, filed June 28, 2001 | |
| CD | | Related U.S. Patent Application Serial No. 09/893,868, filed June 29, 2001 | |

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